AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A semiconductor device comprising:

a memory unit;

a selecting signal terminal for receiving a memory unit selecting signal which is common to a plurality of memory units; and

an identifying unit which includes ~~at least~~ a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal, and an identifier generating circuit, wherein the identifier generating circuit is an adder circuit for carrying the identifier of the memory unit by a half bit and [[for]] generating identifiers for other memory units ~~on the basis of the identifier~~.

2. (Canceled)

3. (Currently amended) The semiconductor device of claim 1, wherein the identifier is one bit data or a plurality of bit data~~, and the identifier generating circuit is an adder circuit for carrying the identifier data of the memory unit bit by bit~~.

4. (Canceled)

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5. (Original) The semiconductor device of claim 1, wherein the identifier generating circuit is electrically connected to a standard voltage power supply for a circuit system or a circuit operation power supply, and the standard voltage power supply voltage or the circuit operation power supply is used as the identifier.

6. (Previously presented) The semiconductor device of claim 1, wherein the memory unit selecting circuit is a comparator for comparing the identifier with the memory unit selecting signal.

7. (Original) The semiconductor device of claim 1, wherein the memory unit is either a DRAM or a SRAM.

8. (Original) The semiconductor device of claim 1, wherein the memory unit is a non-volatile memory which is ROM, EPROM, or EEPROM.

9. (Original) The semiconductor device of claim 1, wherein the selecting signal terminal which receives the memory unit selecting signal is a surplus signal terminal out of address signal terminals which are used for selecting address of the memory unit.

10. (Currently amended) A semiconductor device comprising:

a memory unit;

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a selecting signal terminal for receiving a memory unit selecting signal which is common to a plurality of memory units; and

an identifying unit which is provided outside the memory unit and includes ~~at least~~ a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned thereto and a memory unit selecting signal, and an identifier generating circuit, wherein the identifier generating circuit is an adder circuit for carrying the identifier of the memory unit by a half bit and [[for]] generating identifiers for other memory units ~~on the basis of the identifier of the memory unit~~.

11. (Original) The semiconductor device of claim 10, wherein the memory unit and the identifying unit are constituted by separate semiconductor chips.

12. (Original) The semiconductor device of claim 11, wherein the semiconductor chips constituting the memory unit and the identifying unit are constituted by separate packages.

13. (Original) The semiconductor device of claim 11, wherein the semiconductor chips constituting the memory unit and the identifying unit are constituted by the same package.

14. (Original) The semiconductor device of claim 11, wherein the selecting signal terminal is provided in the semiconductor chip constituting the identifying unit.

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15. (Currently amended) A semiconductor module comprising:

a first memory unit;

a second memory unit positioned on or by the first memory unit;

a first selecting signal terminal provided in the first memory unit and for receiving a memory unit selecting signal which is common to a plurality of memory units;

a second selecting signal terminal provided in the second memory unit and for receiving the memory unit selecting signal which is common to a plurality of memory units;

a first identifying unit including: ~~at least~~ a first memory unit selecting circuit for selecting the first memory unit on the basis of a first identifier assigned thereto and the memory unit selection signal; and a first identifier generating circuit, wherein the first identifier generating circuit is a first adder circuit for carrying the first identifier of the first memory unit by a half bit and generating a second identifier for the second memory unit ~~on the basis of the first identifier~~; and

a second identifying unit including: ~~at least~~ a second memory unit selecting circuit for selecting the second memory unit on the basis of the second identifier assigned thereto and the memory unit selection signal; and a second identifier generating circuit, wherein the second identifier generating circuit is a second adder circuit for carrying the second identifier of the second memory unit by a half bit and generating a third identifier for a third memory unit ~~on the basis of the second identifier~~.

16. (Canceled)

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17. (Original) The semiconductor module of claim 15, wherein the first identifier generating circuit is electrically connected to a standard voltage power supply for a circuit system or a circuit operation power supply, and the standard voltage power supply or the circuit operation power supply is used as the first identifier.

18. (Previously presented) The semiconductor module of claim 15, wherein the first memory unit selecting circuit is a comparator for comparing the first identifier and the memory unit selecting signal, and the second memory unit selecting circuit is a comparator for comparing the second identifier and the memory unit selecting signal.

19. (Original) The semiconductor module of claim 15, wherein the second memory unit is stacked on the first memory unit.

20. (Original) The semiconductor module of claim 15, wherein the second memory unit is juxtaposed to the first memory unit.

21. (Original) The semiconductor module of claim 15 further comprising at least one memory unit and at least one identifying unit.

22. (Currently amended) A semiconductor device comprising:

a memory unit;

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a selecting signal terminal for receiving a memory unit selecting signal which is common to a plurality of memory units; and

an identifying unit ~~at least~~ including an identifier generating circuit provided with ~~at least~~ a fuse element and a resistor element, wherein the resistor element has a resistance value which is higher than a resistance value of the fuse element for generating an identifier assigned to the memory unit, and a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned thereto and the memory unit selecting signal.

23. (Currently amended) The semiconductor device of claim 22, wherein: ~~the identifier generating circuit further includes a resistance element;~~ the fuse element has one end thereof electrically connected to a standard voltage power supply for a circuit system and the other end thereof electrically connected to the memory unit selecting circuit and one end of the resistance element; and the resistance element has the other end thereof electrically connected to the circuit operation power supply for the circuit system.

24-26. (Canceled)

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